AN ACTIVE SUBSTRATE DRIVER FOR MIXED-VOLTAGE SOI SYSTEMS ON A CHIP

Scott A. Jackson[1], *Benjamin J. Blalock*[1], *Mohammed M. Mojarradi*[2], *Harry W. Li*[3]

Microsystems Prototyping Laboratory, Mississippi State University[1]
Mississippi State, MS 39762 U.S.A.
scott@erc.msstate.edu
Jet Propulsion Laboratory, California Institute of Technology[2],
University of Idaho[3]

ABSTRACT

High-voltage transistors in SOI that coexist with traditional low-voltage transistors enable the development of mixed-voltage (high-voltage and low-voltage) systems-on-a-chip. The parasitic back-channel transistor, however, is a critical issue in these mixed-voltage single-chip systems. The presence of high-voltage can create a situation in which the parasitic back-channel device turns on and "shorts-out" the top device inducing functional failure of the system. An active substrate driver has been designed that automatically adjusts the substrate bias voltage to a level insuring the back-channel devices remain off. The active substrate driver should also help compensate for shifts in back-channel transistor threshold voltages induced by temperature, aging, and irradiation effects

I. INTRODUCTION

Fully integrated systems-on-a-chip that include, for example, MEMS-based sensors and actuators, analog-to-digital interfaces, and digital signal processing can require multiple supply voltages. These supplies will range from low voltages, 3.3V or lower, to high voltages, 40V or higher. High voltage transistors have been developed in SOI that can withstand the high supply voltage requirement [1]. A challenge arises when implementing high voltage transistors that coexist with low voltage transistors on the same silicon substrate. These high voltage transistors can withstand drain to source voltages as high as 90V. With such high voltages, a parasitic back-channel device of low-voltage transistors can turn on. Figure 1 illustrates a low-voltage transistor with its parasitic back-channel device [2,3].

If the source or drain of the low-voltage FET is connected to a high voltage node, an inversion layer can form just above the buried-oxide (BOX) allowing current to flow. For the technology used in this work, a partially depleted SOI process, the threshold voltage for an *n*-type

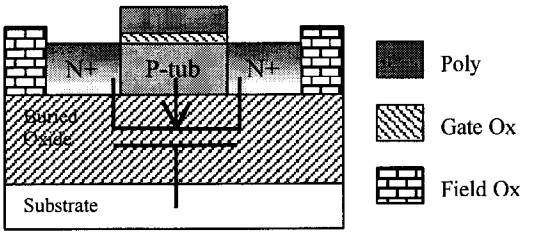

Figure 1. Parasitic Back-channel

back-channel FET ($V_{TN\text{-}BC}$) is approximately 28V and the threshold voltage for a *p*-type back-channel FET ($V_{TP\text{-}BC}$) is approximately –18V. With these threshold voltages, if an appropriate maximum power supply voltage is chosen, the substrate can be biased to a voltage insuring that both the *n*-type and *p*-type back-channel devices are always off.

SOI technology is attractive for those applications requiring radiation hardness such as space exploration. However, as radiation exposure causes positive charge to become trapped in the buried oxide, the parasitic back-channel threshold voltages will lower. If the substrate is

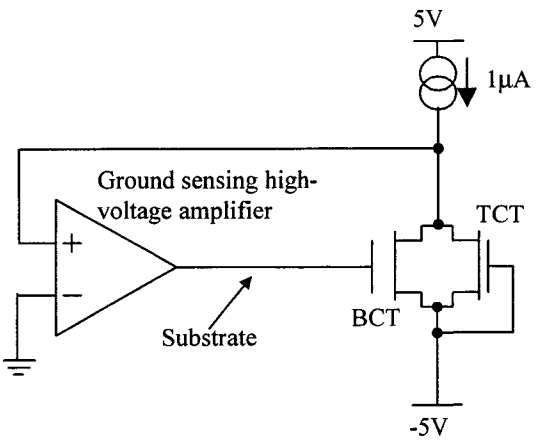

Figure 2. Active substrate driver architecture

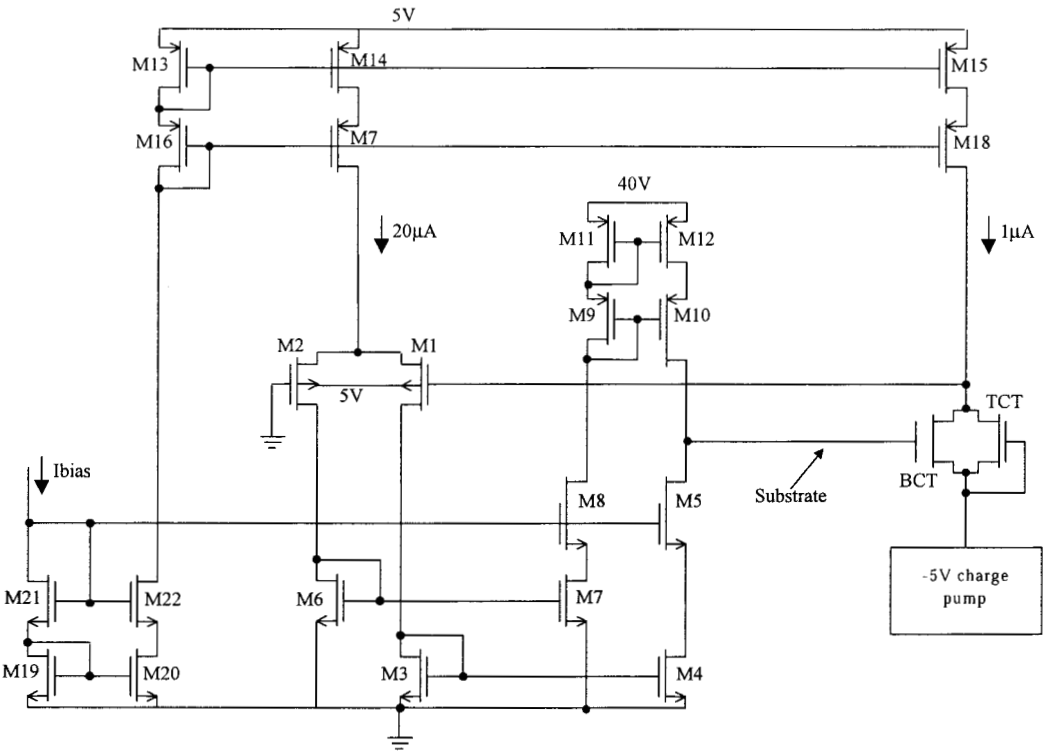

Figure 3. Schematic of Active Substrate Driver

biased with a fixed voltage, the back-channel threshold voltages can shift enough such that the back-channel V_{GS} is greater than the new $V_{TN\text{-}BC}$, causing the *n*-type back-channel device to turn on. To compensate for this an active substrate driver has been developed that will track the change in $V_{TN\text{-}BC}$ and adjust the substrate voltage bias to follow this change

II. CIRCUIT DESCRIPTION

The active substrate driver is illustrated in Figure 2. A 1μA current is forced through an *n*-type back-channel transistor (BCT). The source of this BCT is biased to negative 5V, insuring that its gate-source voltage is 5V greater than any other *n*-type BCT on the chip. Feedback will force this V_{GS} to a level allowing 1μA current to flow in this one BCT. This V_{GS} will be slightly larger than $V_{TN\text{-}BC}$, forcing the substrate voltage to be approximately 5V less than the $V_{TN\text{-}BC}$ of all other n-channel BCTs on the chip. With high levels of irradiation, both $V_{TN\text{-}BC}$ and $V_{TP\text{-}BC}$ will shift in the same direction by approximately the same amount. The active substrate driver will shift the substrate voltage by the same amount, keeping all *n*-type and *p*-type back-channel devices off.

By design, the amplifier's input common-mode range provides ground sensing. The amplifier's output stage can provide a high-voltage output (approximately 2V to 38V). Note also that the amplifier directly drives the substrate. Since the substrate to ground capacitance can vary significantly with buried oxide thickness and die size, the stability requirements of the amplifier take into account substrate capacitance ranging from 10pF to 100pF.

A simplified schematic of the active substrate driver is shown in Figure 3. A charge-pump is used to provide the –5V supply. The amplifier has a low-voltage input stage (5V) and a high-voltage output stage (40V). The low-voltage input stage is used to reduce the number of high-voltage devices needed in the design. This minimizes the circuit's required silicon area since the high-voltage transistors occupy significantly more area than low-voltage transistors. A *p*-channel source-coupled input pair is used to provide the ground-sensing capability. Devices M5, M8, and M10 are high voltage transistors. These transistors are not self-aligned and have poor matching; therefore, low voltage transistors are used to enhance input/output current matching in the current mirrors M3-M5, M6-M8, and M9-M12.

The –5V charge pump is illustrated in Figure 4. Cascading two identical charge pumps, which are compliments of the charge pump found in [4], generates

the –5V needed at the source of the BCT. The circuit is clocked by a 1MHz 5V square-wave. The first stage produces an output of approximately –3.2V. The second stage produces –5.2V with no load and –4.8V with a 1μA load.

III. SIMULATION

The active substrate driver is simulated in a 0.8μm partially-depleted SOI technology. BSIM3v3 device models are utilized. Figure 5 shows simulation data of the active substrate driver driving a substrate with a 10pF capacitance. The waveforms correspond to the startup condition with the 5V supply ramping from 0V to 5V in 30μS and the 40V supply ramping to 40V in 300μs. The substrate voltage reaches its quiescent point within approximately 175μs. At this point 1μA flows through the BCT which causes the feedback node from the drain of the BCT to reach a stable value of approximately 0V. The charge pump output voltage changes from –5.2V to –4.8V at this time as well. After reaching a stable state, the active substrate driver tracks changes in V_{TN-BC}.

IV. CONCLUSIONS

While consuming 61μA of current, the active substrate driver maintains a phase margin between 80 degrees and 95 degrees for the capacitance loads given above. With a 10pF load, the active substrate driver requires approximately 170μs to reach its quiescent point after startup. With a 100pF load, 220μs is required. After the startup quiescent point is reached, changes in the back-channel threshold voltages are very slow with respect to time (essentially DC) and the active substrate driver can easily track to compensate for such changes. The active substrate driver enables the implementation of mixed-voltage systems-on-a-chip in partially-depleted SOI technology.

ACKNOWLEDGEMENTS

The work described in this paper was carried out for the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

REFERENCES

[1] T. W. Johnson, "A High-Voltage Half-Bridge in 1.2 μm CMOS Process," (Master Thesis, School of EE and CS, Washington State University, 1998).

[2] M. M. Mojarradi *et al.*, "Power Management and Distribution for System on a Chip For Space Applications," 1999 AIAA Space Technology Conference & Exposition. Albuquerque, New Mexico.

[3] S. T. Liu, W. C. Jenkins, and H. L. Hughes, "Radiation Response of SOI Materials," Electromechanical Society proceedings, vol. 99-3, pp. 225-231, 1999.

[4] P. Favrat, *et al.*, "A High-Efficiency CMOS Voltage Doubler," J. Solid State Circuits, vol. 33, pp. 410-416, March 1998.

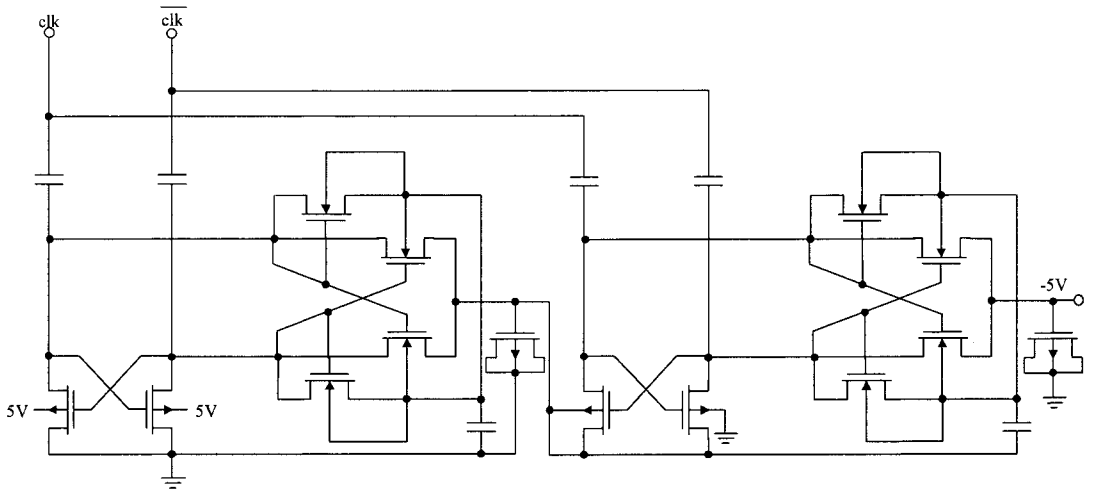

Figure 4. –5V charge pump.

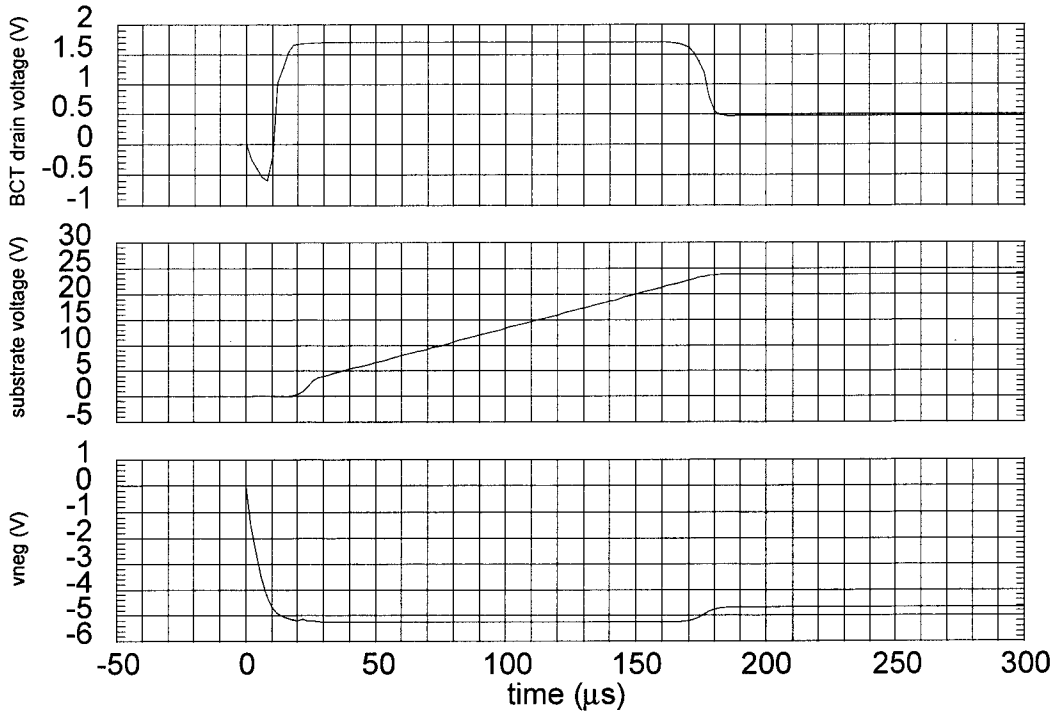

Figure 5: Simulation Results